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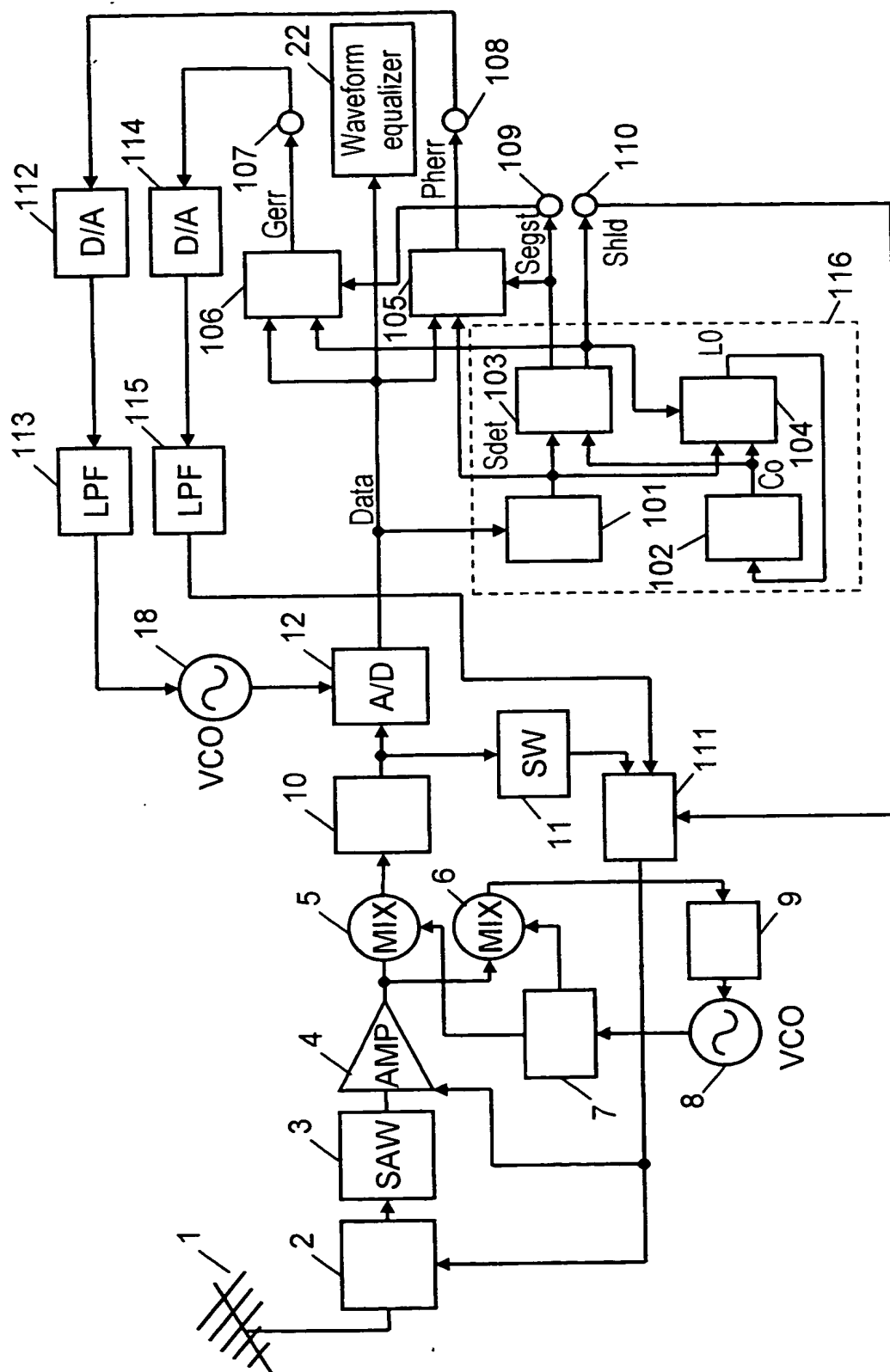
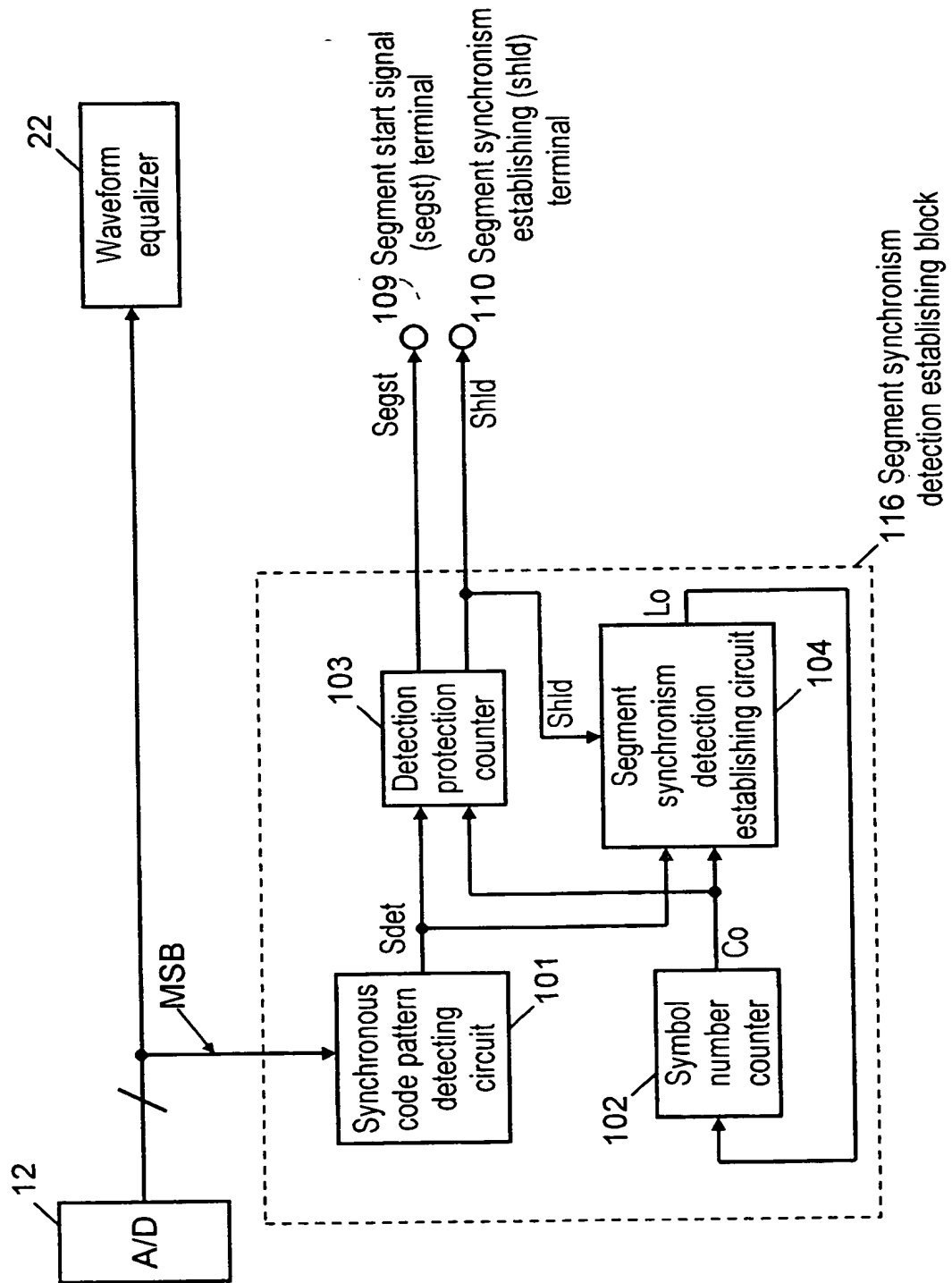


FIG.2



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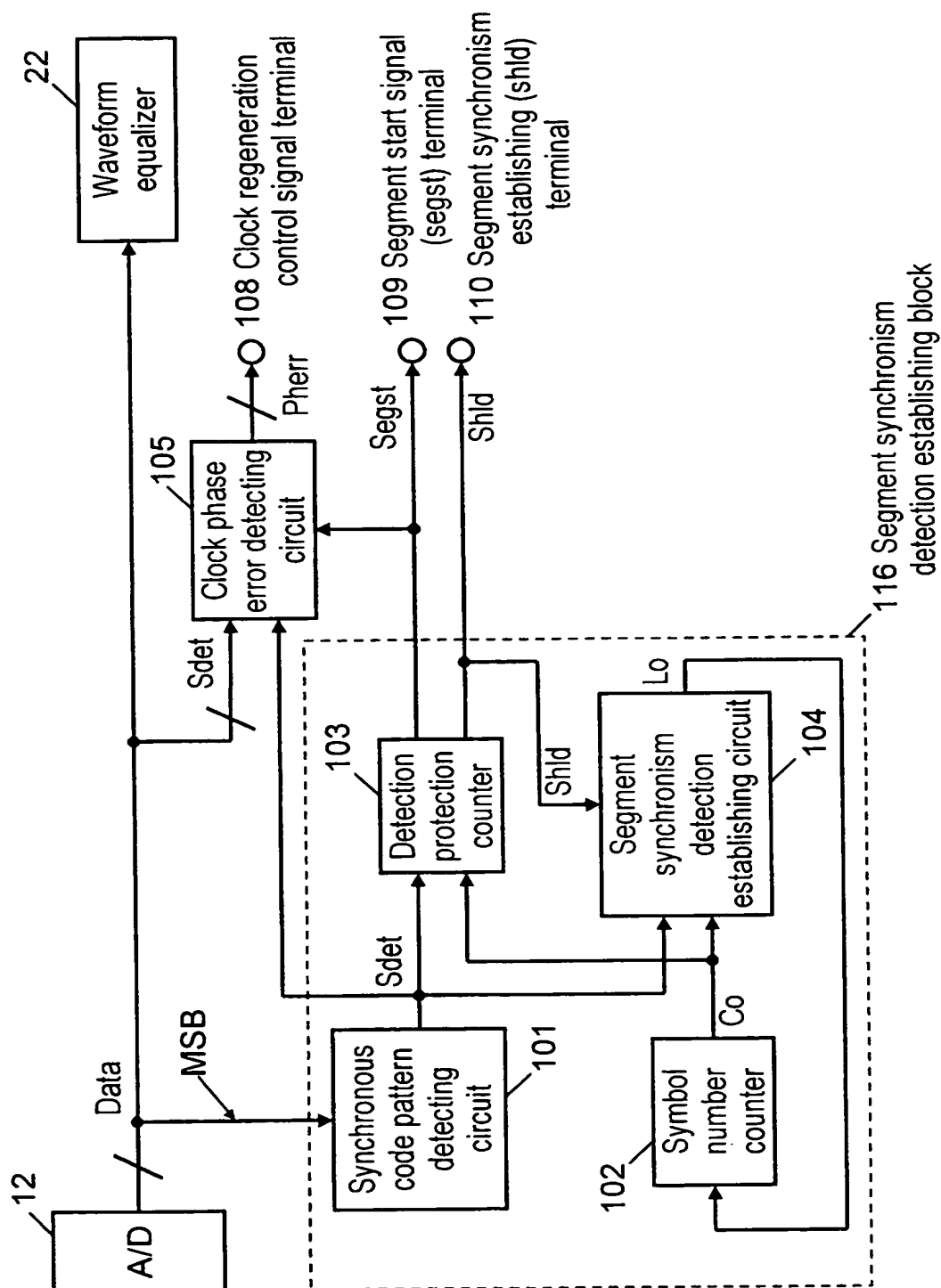


FIG. 4

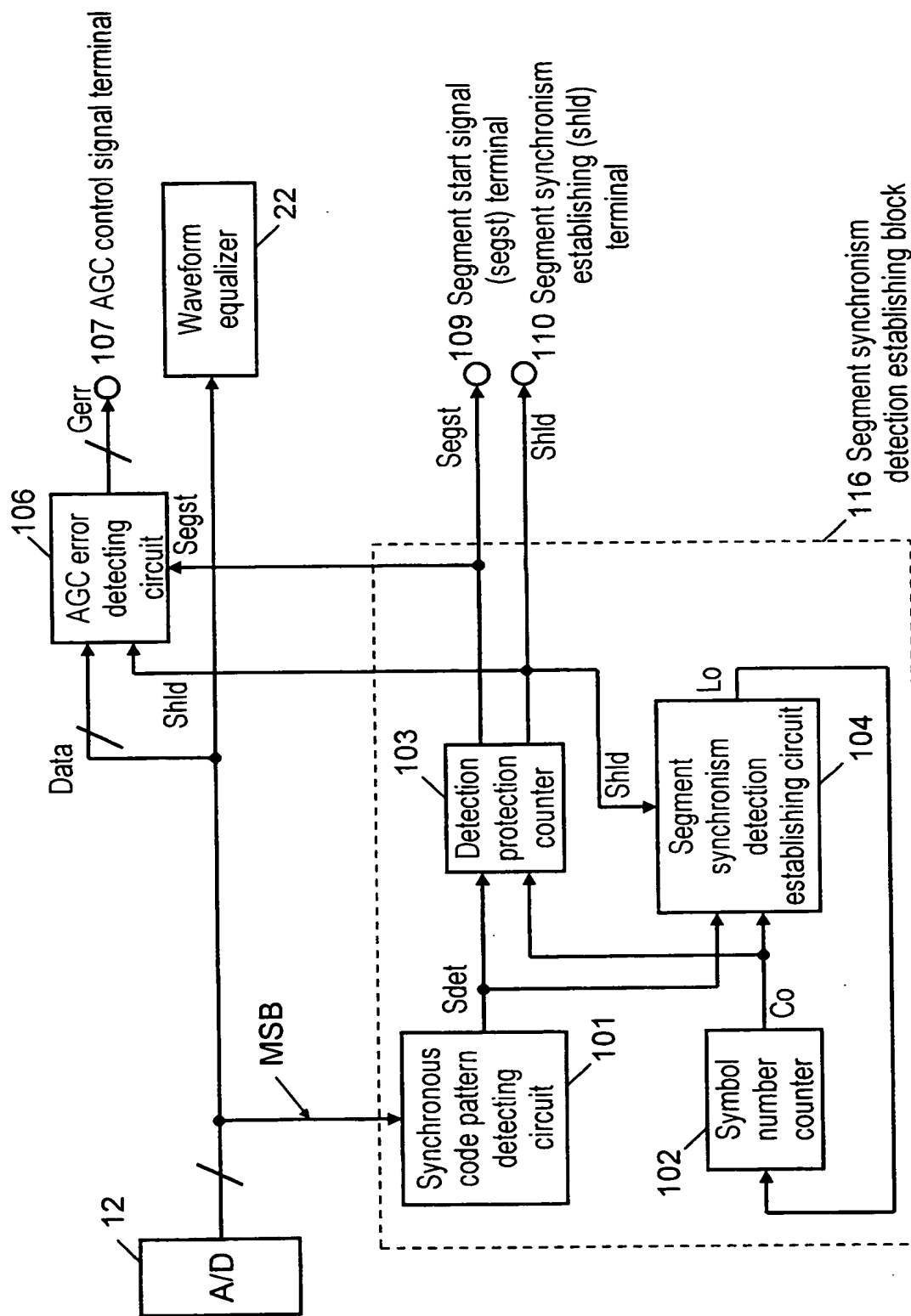
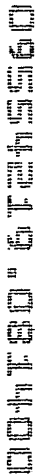
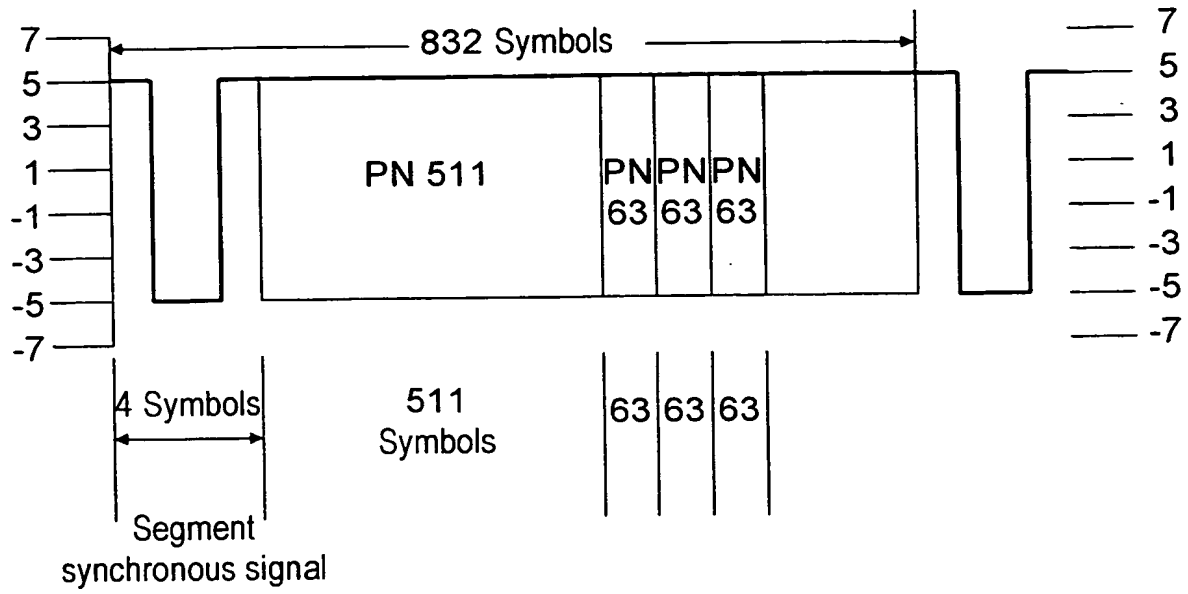


FIG. 5



6/12

FIG. 6



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7/12

FIG. 7

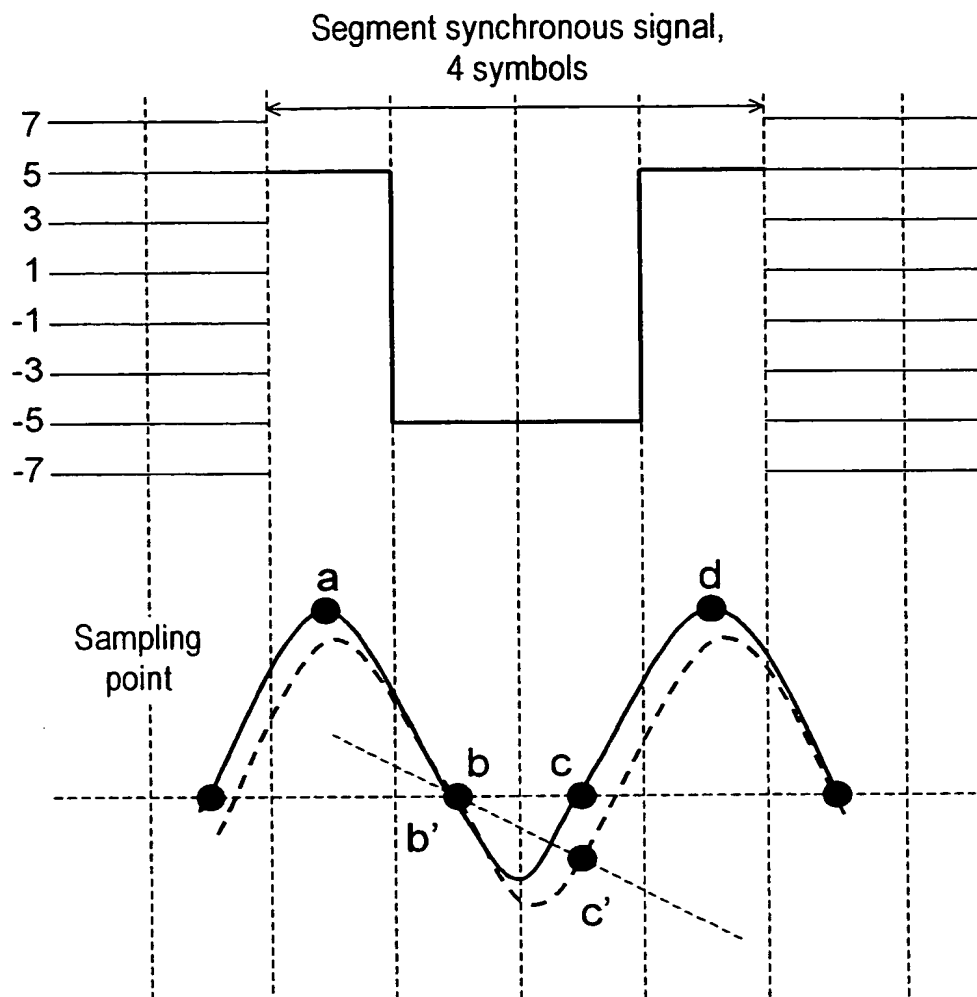
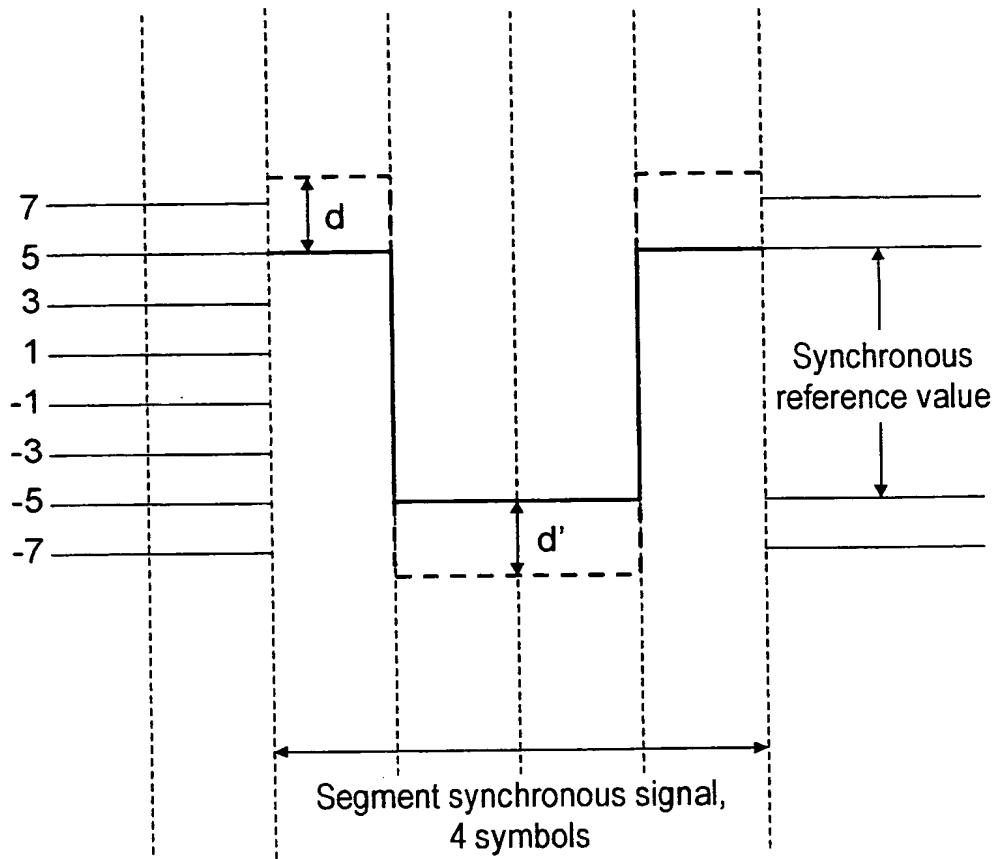


FIG. 8



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FIG. 9

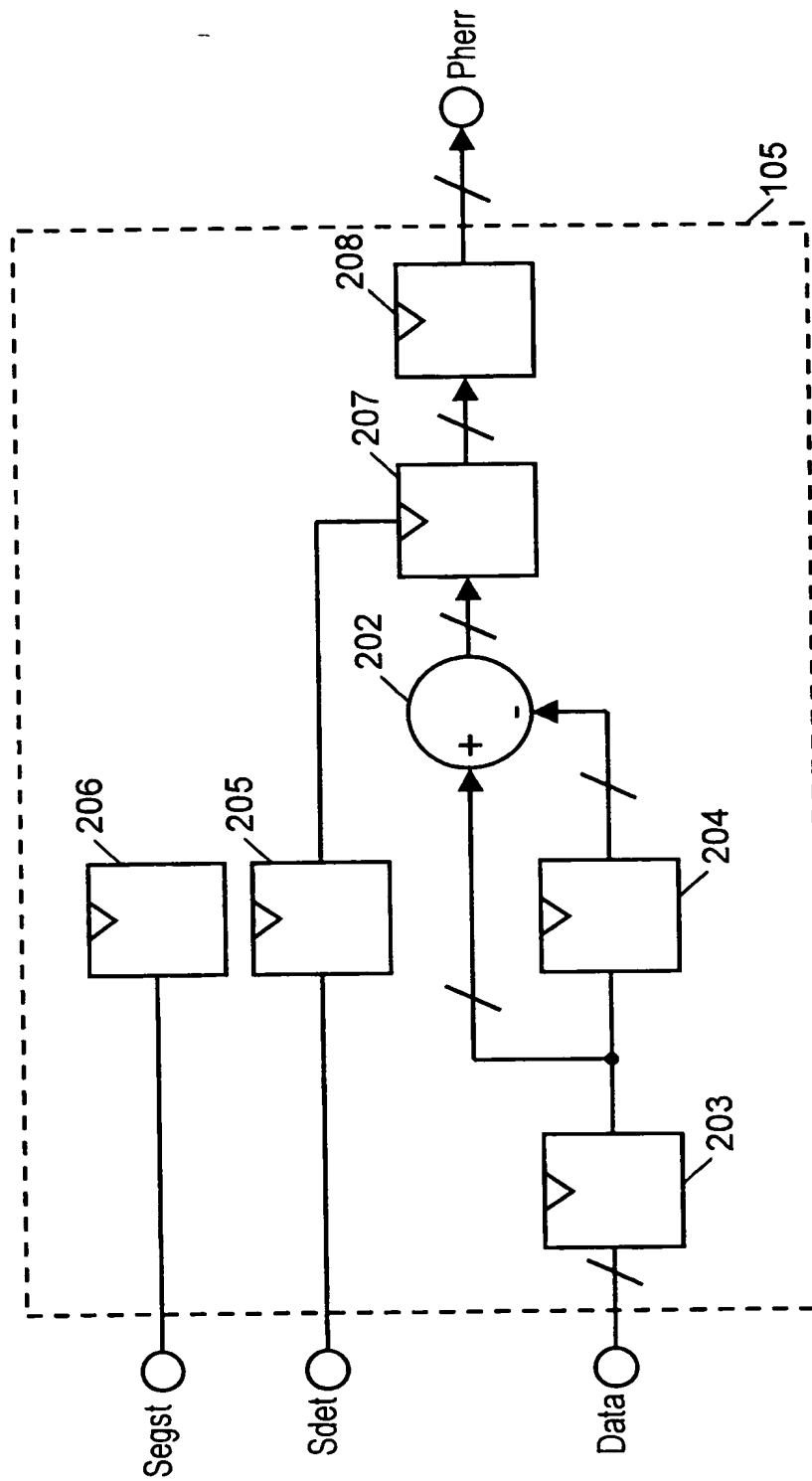
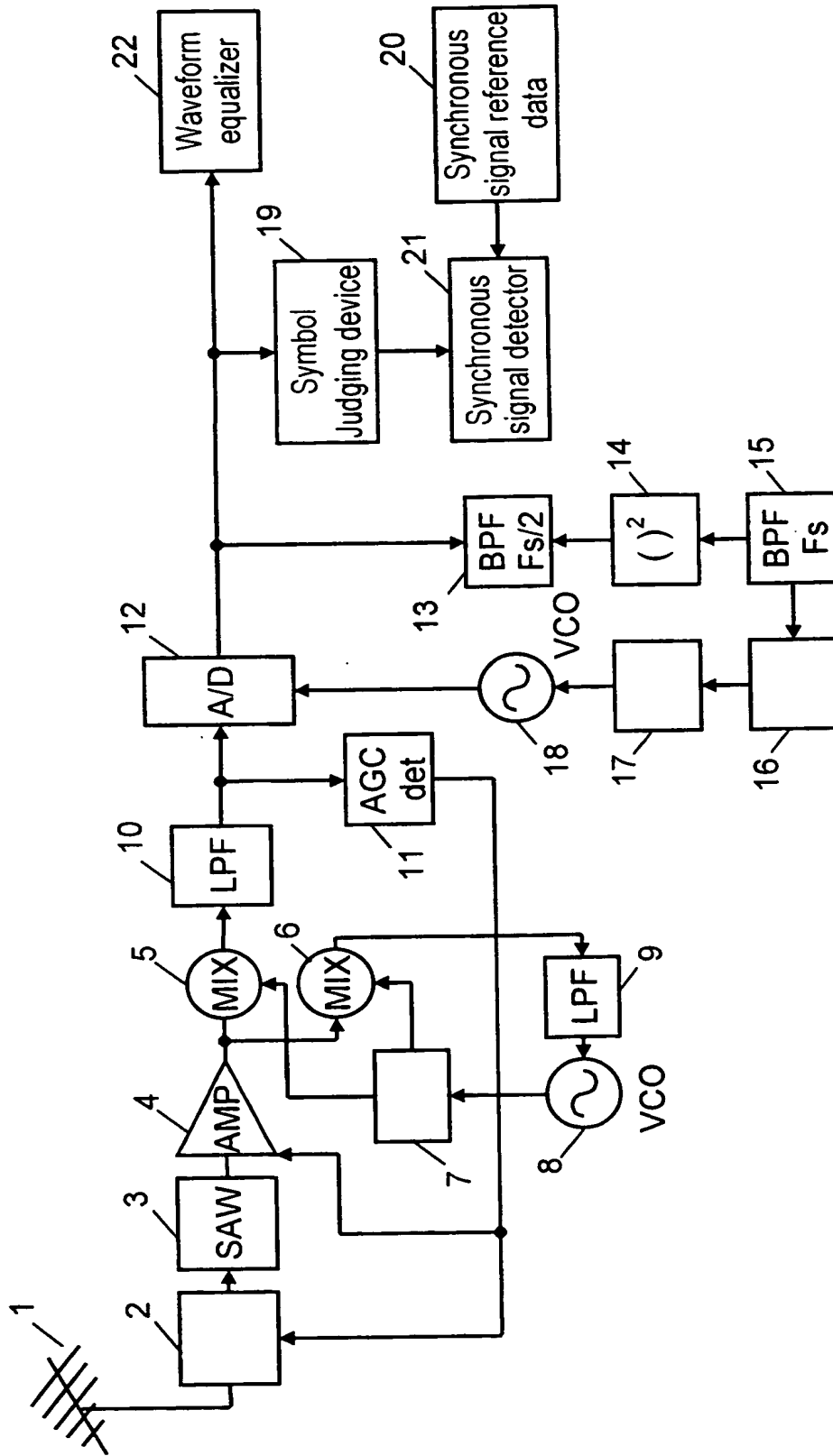


FIG. 10



Reference	Numerals
1	Reception antenna
2	Digital broadcast tuner
3	SAW filter
4	Analog amplifier for amplifying
5, 6	Mixer
7	90-degree phase shifter
8, 18	Voltage control oscillator (VCO)
9, 10	Low pass filter (LPF)
11	AGC detector for detecting signal
12	A/D converter
13	Band pass filter for passing 1/2 of symbol speed
14	Square circuit
15	Band pass filter for passing symbol speed $f_s$
16	Phase detector for detecting
17	Loop filter
19	Symbol judging device
20	Synchronous signal reference
21	Synchronous signal detector
22	Waveform equalizer
101	Synchronous code pattern detector
102	Symbol number counter
103	Detection protection counter
104	Segment synchronism detector
105	Clock phase error detecting
106	AGC error detecting circuit
107	AGC control signal terminal
108	Clock regeneration control

- 1 Reception antenna
- 2 Digital broadcast tuner
- 3 SAW filter
- 4 Analog amplifier for amplifying signal
- 5, 6 Mixer
- 7 90-degree phase shifter
- 8, 18 Voltage control oscillator (VCO)
- 9, 10 Low pass filter (LPF)
- 11 AGC detector for detecting signal envelope
- 12 A/D converter
- 13 Band pass filter for passing frequency component of  
1/2 of symbol speed
- 14 Square circuit
- 15 Band pass filter for passing frequency component of  
symbol speed  $F_s$
- 16 Phase detector for detecting phase error
- 17 Loop filter
- 19 Symbol judging device
- 20 Synchronous signal reference data
- 21 Synchronous signal detector
- 22 Waveform equalizer
- 101 Synchronous code pattern detecting circuit
- 102 Symbol number counter
- 103 Detection protection counter
- 104 Segment synchronism detection establishing circuit
- 105 Clock phase error detecting circuit
- 106 AGC error detecting circuit
- 107 AGC control signal terminal
- 108 Clock regeneration control signal terminal

12/12

109 Segment start signal (Segst) terminal  
110 Segment synchronism establishing (Shld) terminal  
112, 114 D/A converter  
113, 115 LPF  
116 Segment synchronism detection establishing block  
202 Subtractor  
203, 204, 205, 206, 207, 208 Latch  
Co Count-up signal  
Data Digital data  
Gerr Error signal  
Lo Output signal  
MSB Most significant bit  
Pherr Clock regeneration control signal  
Sdet Code pattern detection signal  
Segst Segment start signal  
Shld Segment synchronism establishing signal

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